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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
RICHARDS, N DREW	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/074,732
Filing Date: February 13, 2002
Appellant(s): MATHEW ET AL.

MAILED
SEP 2 2 2005
GROUP 2800

Robert L. King
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/30/05 appealing from the Office action mailed 12/10/04.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,472,258 B1	ADKISSON ET AL.	10-2002
2003/0113970	FRIED ET AL.	6-2003
6,097,065	FORBES ET AL.	8-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 2, 4, 5, 7 – 12, 14, 16 – 25, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (USPAT 6472258, Adkisson) in view of Fried et al. (USPUB 2003/0113970, Fried).

With regard to claim 1, Adkisson discloses in figures 1 – 5 a method of forming a vertical double gate semiconductor device. Adkisson discloses in figure 1 providing a

semiconductor substrate (10). Adkisson discloses in figure 1 providing a first insulating layer (12) over the semiconductor substrate. Adkisson discloses in figure 1 providing a first semiconductor layer (14) over the first insulating layer. Adkisson discloses in figures 1 and 2, and column 3, lines 3 – 37 removing portions of a first semiconductor layer to form the semiconductor structure having a first sidewall (left side of the middle Si region) and a second sidewall (right side of the middle Si region), wherein the first sidewall is opposite the second sidewall. Adkisson discloses in figure 2 forming a second insulating layer (gate oxide) adjacent the first sidewall and the second sidewall. Adkisson discloses in figure 2 and column 3, lines 41 – 48 providing a second semiconductor layer (20) over and adjacent the semiconductor structure, the second semiconductor layer being elevated in an area overlying the semiconductor structure (not shown: after deposition and before the polishing and recessing steps) and having a non-horizontal surface adjoining the semiconductor structure (vertical surfaces of gate polysilicon sandwiching the gate oxide with the semiconductor structure). Adkisson discloses in figure 2 and column 3, lines 41 – 48 wherein the second semiconductor layer is conductive. Adkisson does not teach implanting the second semiconductor layer in a first area adjacent the semiconductor structure with a first species and implanting the second semiconductor layer in a second area with a second species. Fried teaches in figure 2b, figure 3b, and paragraph 0031 performing a first directional implant (20) of a first conductivity type (n-type) of a second semiconductor layer (18) from a first predetermined direction. Fried further teaches in figure 3b and paragraph 0031 performing a second directional implant (22) of a second conductivity type (p-type)

opposite the first conductivity type of the second semiconductor layer from a second predetermined direction. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the double doping process of Fried in the method of Adkisson in order to make the second semiconductor layer conductive and shift the threshold voltage of the device to be compatible with current state of the art CMOS technology as stated by Fried in paragraph 0007. It is further obvious that the implanting step of Fried must be accomplished before the polishing and recessing steps of Adkisson in order to dope gate electrodes without counterdoping. Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, column 3, line 61 – column 4, line 24, and column 4, line 65 – column 5, line 12 forming a conductive layer (42 and 50) over the semiconductor structure and the second insulating layer. Adkisson discloses in figure 2 and column 3, lines 40 – 49 removing a portion of the second semiconductor layer to physically separate a first gate region (the region to the right of the first semiconductor) and a second gate region (the region to the left of the first semiconductor). Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, column 3, line 61 – column 4, line 24, and column 4, line 65 – column 5, line 12 removing a portion of the conductive layer. Adkisson discloses in figure 2 wherein the first gate region is adjacent the first sidewall of the semiconductor structure, and it would have been further obvious in view of Fried that the first gate region would have the first conductivity type. Adkisson discloses in figure 2 wherein the second gate region is adjacent the second sidewall of the semiconductor structure, and it would have been further obvious in view of Fried that the second gate region would have the second conductivity type. It should be noted that

the claim limitation "the semiconductor structure preventing migration of doping species between the first gate region and the second gate region" is an intended use recitation that is met by the combination of Adkisson and Field.

With regard to claim 2, Adkisson discloses in figure 2 and column 3, lines30 – 36 wherein the semiconductor structure is a channel region of the vertical double gate semiconductor device.

With regard to claim 4, Adkisson discloses in figure 2 and column 3, lines 40 – 49 wherein removing the portions of the second semiconductor layer comprises planarizing the conductive layer. Adkisson discloses in figure 5, and column 4, line 65 – column 5, line 12 wherein removing the portions of the conductive layer comprises planarizing the conductive layer.

With regard to claim 5, Adkisson discloses in figure 3a further comprising forming a first current electrode region (right end of first semiconductor layer as seen in the shape resembling an "H") and a second current electrode region (left end of first semiconductor layer)in the semiconductor substrate to implement the vertical double gate semiconductor device as a transistor.

With regard to claim 7, Fried teaches in figure 3b and paragraph 0031 each of the first directional implant and the second directional implant is performed by ion implantation at symmetric opposing angles relative to a top surface of the semiconductor substrate.

With regard to claim 8, Fried teaches in paragraph 0032 further comprising annealing the first gate region and the second gate region after the first directional implant and the second directional implant.

With regard to claim 9, Adkisson teaches in figure 2 and column 3, lines 41 – 49 removing a portion of the conductive layer. It is not clear if Adkisson and Fried teach wherein removing a portion of the conductive layer is performed after performing the first directional implant. It would have been obvious in the method of Adkisson and Fried that the conductive layer would be removed only after performing the first directional implant because the second semiconductor of Adkisson is only referred to as gate material. An intrinsically deposited polysilicon would not be sufficient to act as a gate material of the device in Adkisson, and therefore must be made conductive by implanting and doping through the method of Fried. Therefore, in the method of Adkisson and Fried, the conductive layer would not be formed until after the implantation steps are performed to make the gate material conductive.

With regard to claim 10, Adkisson discloses in figure 3 and column 4, lines 14 – 17 further comprising electrically coupling the first gate region and the second gate region (before etching to form spacers, the gate regions are coupled).

With regard to claim 11, Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, column 3, line 61 – column 4, line 24, and column 4, line 65 – column 5, line 12 further comprising forming a metal layer as the conductive layer.

With regard to claim 12, Adkisson discloses in figure 5, and column 4, lines 14 – 23 wherein forming the conductive layer comprises forming a silicon layer (layer of

polysilicon in column 4, lines 20 – 21) over the first electrode region, the second electrode region, and the semiconductor structure. Adkisson discloses in figure 5, and column 4, lines 14 – 23 forming a first metal layer (silicide of column 4, line 14) over the silicon layer. Adkisson does not teach heating the semiconductor substrate so that the silicon layer and the first metal layer form a silicide. Salicide processing is a well known technique to form silicide layers. Fried teaches in figures 3b, figure 4b, and paragraph 0032 a salicide technique for forming silicide layers. Fried teaches in figures 3b, figure 4b, and paragraph 0032 wherein forming the forming a first metal layer over a silicon layer (28). Fried teaches in figures 3b, figure 4b, and paragraph 0032 heating the semiconductor substrate (10b) so that the silicon layer and the first metal layer form a silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the salicide process of Fried in the method of forming a silicide of Adkisson in order to create a contact that has no abrupt electrical barrier between it and the electrode. Such a contact provides superior electrical connection as is well known in the art.

With regard to claim 13, Adkisson discloses in figure 3, figure 3b, and column 4, lines 16 – 17 removing a portion of the conductive layer to form a first contact for the first electrode region and a second contact for the second electrode region, wherein the first contact and the second contact are electrically isolated from each other.

With regard to claim 14, Adkisson discloses in figures 5 and 5a and column 4, lines 65 – column 5, line 12 wherein removing a portion of the conductive layer comprises planarizing (damascene and conventional contacts) the conductive layer.

With regard to claim 16, Adkisson discloses in figure 3, and column 4, lines 20 – 24 wherein the metal layer further comprises a stack of metal layers (42 and 50).

With regard to claim 17, Adkisson discloses in figures 1 – 5 a method of forming a vertical double gate semiconductor device. Adkisson discloses in figure 1 providing a semiconductor substrate (10). Adkisson discloses in figure 1 forming a first insulating layer (12) over the semiconductor substrate. Adkisson discloses in figure 1 forming a first semiconductor layer (14) on the first insulating layer. Adkisson discloses in figures 1 and 2 etching portions of the first semiconductor layer to form a semiconductor structure (Si) having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction. Adkisson discloses in figures 1 – 3a and column 2, lines 48 – 57 forming a source region and a drain region in the semiconductor substrate in a second direction, wherein the first direction is substantially perpendicular the second direction. Adkisson discloses in figure 2 forming a second insulating layer on the first sidewall and the second sidewall. Adkisson discloses in figure 2 and column 3, lines 40 – 49 forming a second semiconductor layer (20) over and adjacent the semiconductor structure and the second insulating layer. Adkisson discloses in figure 2 and column 3, lines 41 – 49 wherein the second semiconductor layer comprises (before polishing and recessing steps disclosed in figure 3, lines 41 – 42) a first semiconductor portion which is adjacent the first sidewall and having a first non-horizontal (vertical) surface, a second semiconductor portion (not shown, before polishing) which is over the semiconductor structure, and a third semiconductor portion which is adjacent the second sidewall and having a second non-horizontal (vertical) surface. Adkisson

discloses in figure 2, and column 3, lines 40 – 49 that the gate polysilicon is conductive in order for the device to be capable of working as a semiconductor device. Adkisson does not teach doping by an angular implant the first semiconductor portion and the third semiconductor portion. Fried discloses in figure 3b, and paragraph 0031 doping (20) a first semiconductor portion (24) with a first species and doping (22) a third semiconductor portion(26) with a second species opposite the first species. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the doping of Fried in the method of Adkisson in order to make the second semiconductor layer conductive and shift the threshold voltage of the device to be compatible with current state of the art CMOS technology as stated by Fried in paragraph 0007. Adkisson discloses in figure 2, and column 3, lines 40 – 49 removing the second semiconductor portion. It would have been further obvious in the method of Adkisson and Fried the removing the second semiconductor portion would be subsequent to forming the first and second semiconductor portions because the third portion is needed in the formation of the first and second portions and the removal will serve to physically separate the first semiconductor portion and the third semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and the third semiconductor portion, the semiconductor structure comprising differing material composition than the first semiconductor portion and the third semiconductor portion at all adjoining surfaces.

With regard to claim 18, Adkisson discloses in column 3, lines 37 - 40 wherein the second insulating layer is deposited conformally (deposited).

With regard to claim 19, Fried teaches in paragraph 0032 further comprising annealing the second semiconductor layer.

With regard to claim 20, Adkisson teaches in figure 2 and column 3, lines 41 – 49 removing the second semiconductor portion. It is not clear if Adkisson and Fried teach wherein removing the second semiconductor portion is performed after doping the second semiconductor layer. It would have been obvious in the method of Adkisson and Fried that the second semiconductor portion would be removed only after the annealing because the second semiconductor of Adkisson is only referred to as gate material. The deposited polysilicon of Fried would not be sufficient to act as a gate material of the device in Adkisson until the layer is conductive enough to be a gate polysilicon. Therefore, the gate polysilicon must be annealed in the method of Adkisson and Fried before removal of the second semiconductor portion because the annealing is part of forming the gate polysilicon.

With regard to claim 21, Adkisson discloses in column 3, lines 40 – 49 wherein removing the second portion is performed by planarization (polished).

With regard to claim 22, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion further comprises doping the first semiconductor portion with a first species and doping the third semiconductor portion with a second species, wherein the first species and the second species are different in conductivity.

With regard to claim 23, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion is performed

by ion implanting species at an angle relative to a top surface of the semiconductor substrate.

With regard to claim 24, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion further includes forming a patterned layer (14) over the semiconductor substrate.

With regard to claim 25, Adkisson discloses in figures 1 and 2; and column 3, lines 20 – 30 wherein etching portions of the first semiconductor layer to form the semiconductor structure further comprises: forming a third insulating layer (thin oxide) over the first semiconductor layer; forming a nitride layer (SiN) over the third insulating layer; patterning the nitride layer and the third insulating layer; and etching the first semiconductor layer using the nitride layer and the third insulating layer as a mask.

The rejection of claim 34 is similar to the rejection of claims 1 and 17 above using Adkisson in view of Fried.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson and Fried as applied to claims 1 and 11 above, and further in view of Forbes et al. (USPAT 6414356, Forbes).

With regard to claim 15, Adkisson discloses in figures 2 – 3 forming first and second gate regions before forming the metal. Adkisson does not teach further comprising annealing the first gate region and the second gate region before forming the metal. Forbes teaches in figure 4L, figure 4M, figure 5a, column 12, lines 29 – 55, and column 13, lines 16 – 61 annealing a first gate region (463a) and a second

electrode region (463b) before forming a metal (560). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the annealing of Forbes in the method of Adkisson and Fried in order to activate dopant species in the gate layer as stated by Forbes in column 12, lines 35 – 55.

(10) Response to Arguments

Response to arguments for Ground I:

Independent Claim 1

Appellant argues that Adkisson et al. has no teaching of "providing a second semiconductor layer over and adjacent the semiconductor structure, the second semiconductor layer being elevated in an area overlying the semiconductor structure and having a non-horizontal surface adjoining the semiconductor structure" as recited in claim 1. This argument is not persuasive.

First, Adkisson clearly show in figure 2 that the second semiconductor layer 20 is adjacent the semiconductor structure (thin vertical Si region) and has a non-horizontal surface adjoining the semiconductor structure (vertical surfaces of gate polysilicon sandwiching the gate oxide with the semiconductor structure). Adkisson does not clearly depict the second semiconductor layer being over the semiconductor structure and being elevated in an area overlying the semiconductor structure. Nonetheless, this limitation is still taught by Adkisson. To recognize that this limitation is taught, one

needs to look at the entirety of the process Adkisson performs to obtain the structure shown in figure 2.

Adkisson teach on column 3 lines 41-48 that the gate material (polysilicon) 20 is deposited, polished and recessed below the nitride 16 surface. Figure 2 shows the resulting structure after all three steps have been completed, that is after depositing, polishing and recessing the polysilicon gate material. As explained in the rejection, at an intermediate point not shown in the figures after the deposition and before the polishing and recessing steps, the second semiconductor layer 20 is over the semiconductor structure and is elevated in an area overlying the semiconductor structure. One of ordinary skill in the art would recognize that the deposition step initially forms the second semiconductor layer 20 over the entire structure. This deposition would result in a structure where the second semiconductor layer 20 is over the semiconductor structure and is elevated in an area overlying the semiconductor structure. This deposition would be similar to the conventional deposition of polysilicon 18 as shown in figure 2B of Fried et al. (see paragraph 0029 of Fried et al. for a brief discussion of the "conventional" deposition of the polysilicon). The end result of this deposition process gives the structure of the second semiconductor layer as claimed. If the deposition process did not result in this structure having the second semiconductor elevated above the semiconductor structure, then the polishing step of Adkisson could not be performed. Adkisson teach in column 3 lines 45-47 that in the polishing step the nitride serves as a polish stop. Thus, one of ordinary skill in the art would recognize that the second semiconductor material 20 would necessarily be formed elevated above

the semiconductor structure (and nitride cap on the semiconductor structure) in order for the polishing to be performed as taught using the nitride as a polish stop. Thus, in an intermediate point in the process, after the deposition but before the polishing and recessing, Adkisson teach the second semiconductor layer having the structure as recited in claim 1.

Appellant further argues that there is no teaching in Adkisson of "providing a first directional implant of a first conductivity type," "providing a second directional implant of a second conductivity type" or of teaching that the double gates are oppositely doped in conductivity. This argument is not persuasive. Adkisson is not relied upon to teach these claimed features. These steps are taught by Fried and have been properly combined with Adkisson to result in the invention as recited in claim 1. Thus, Adkisson's lack of teaching these features is not persuasive in arguing against the rejection based upon Adkisson in view of Fried. This argument merely attacks Adkisson individually. Nonobviousness cannot be shown by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the combination of Adkisson with Fried as applied and explained in the rejection above, Adkisson with Fried do teach providing the first and second directional implant that results in the double gates being oppositely doped in conductivity.

Appellant further states that there is no teaching or suggestion of using a semiconductor structure for "preventing migration of doping species between the first gate region and the second gate region" as recited in claim 1. This is not persuasive. Though not explicitly recognized by Adkisson or Fried alone, the end result of the combination of their processes (using the first and second opposite conductivity implants of Fried into the process of Adkisson) is that the semiconductor structure prevents migration of the doping species between the first and second gates. Since Adkisson teach removing the portion of the gate material (second semiconductor layer 20) over the semiconductor structure to separate the layer into a first and second gate, the net result is the same as that claimed where the semiconductor structure (which exists between and separates the two gates) prevents the migration of the doping species.

Appellant further argues that Fried et al. do not teach or suggest "removing a portion of the conductive layer and the second semiconductor layer to physically separate a first gate region and a second gate region." This argument is not persuasive since the rejection over the combination of Adkisson with Fried does not rely upon Fried to teach this limitation. Adkisson teach removing a portion of the conductive layer in figures 3, 3a, 5 and 5a as well as in column 3 lines 61 through column 4 line 24 and column 4 lines 65 through column 5 line 12. Adkisson teach removing a portion of the second semiconductor layer to physically separate a first gate region and a second gate region to arrive at the structure of figure 2 in column 3 lines 40-49. Thus, even though

Fried does not teach these steps, they are taught by Adkisson in the rejection over the combination of references. This argument merely attacks Fried individually. Nonobviousness cannot be shown by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant further argues that Fried does not teach or suggest "the semiconductor structure preventing migration of doping species between the first gate region and the second gate region." This is not persuasive. Though not explicitly recognized by Adkisson or Fried alone, the end result of the combination of their processes (using the first and second opposite conductivity implants of Fried into the process of Adkisson) is that the semiconductor structure prevents migration of the doping species between the first and second gates. Since Adkisson teach removing the portion of the gate material (second semiconductor layer 20) over the semiconductor structure to separate the layer into a first and second gate, the net result is the same as that claimed where the semiconductor structure (which exists between and separates the two gates) prevents the migration of the doping species.

Appellant then argues that Adkisson and Fried combined have no teaching or suggestion to prevent the cross-migration of a FINFET having asymmetric gate doping and that any statement saying so is hindsight reconstruction. This is not persuasive.

Neither Adkisson nor Fried need to have a teaching or suggestion to prevent the cross-migration. This feature is a necessary function of the necessary result of the combination of Adkisson and Fried. Adkisson and Fried have been properly combined, using teachings and motivations from the references themselves, to obtain the claimed invention. The fact that neither reference recognizes the problem of cross-migration does not refute the fact that the structure obtained by their combination does prevent the cross-migration.

Appellant further argues that applying the angle implanting of Fried to the structure of Adkisson in figure 2 or 3 would not result in gate regions having a single dopant type. This is not persuasive. This argument is based upon the teaching of Fried that horizontal portions of the gate structure will not be shadowed during either the first or second implant and will thus receive both implants and that since figure 2 of Adkisson only has a horizontal gate structure it will be double implanted. First, as explained in the rejection, it would have been obvious to one of ordinary skill in the art to employ the angled implant of Fried to the intermediate structure of Adkisson after depositing the second semiconductor layer and before polishing and recessing. One would be motivated to employ the implantation of Fried at this point in the process to obtain the advantageous asymmetric gates of Fried. Employing the angled implantation of Fried at the further point in the process shown in Adkisson figure 2 (after polishing and recessing) would ignore the teachings of Fried in using the angled implant specifically to obtain oppositely doped gates. Note that appellant argues that applying the implant of

Fried to the structure of Adkisson figure 2 or 3 would not result in the gate regions having a single dopant type. The examiner does not refute this point. However, the rejection relies upon applying the implant of Fried in Adkisson's process before figure 2, at which point the angled implant will produce the claimed gates. Thus, appellant's argument is not persuasive.

Appellant further argues that the teachings of Fried and Adkisson are very different with respect to gate structure since Fried teach an electrically continuous gate and Adkisson teach a device with electrically separate gates. In response to applicant's argument that Fried and Adkisson are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both Fried and Adkisson are in the field of applicant's endeavor since they both teach forming FINFET devices having a gate on both sides of the fin. Further, neither Fried not Adkisson is considered to teach away from the combination of the two references. Regardless of whether Fried teach two separate gates the same as Adkisson, Fried still gives proper motivation for forming the gates with asymmetric doping to allow a threshold voltage that is compatible with current CMOS circuit designs. Thus, Fried and Adkisson are properly combinable to teach the claimed invention.

Dependent Claims 2, 4, 5, 7-12, 14 and 16

Appellant does not present any further arguments for these dependent claims. The arguments made with regard to claim 1 above apply to these dependent claims and the arguments and the rejection they are in support of are considered proper.

Independent Claim 17

Appellant argues that Adkisson et al. has no teaching of "forming a second semiconductor layer over and adjacent the semiconductor structure and the second insulating layer, wherein the second semiconductor layer comprises: a first semiconductor portion which is adjacent the first sidewall and having a fist non-horizontal surface; a second semiconductor portion which is over the semiconductor structure; and a third semiconductor portion which is adjacent the second sidewall and having a second non-horizontal surface" as recited in claim 17. This argument is not persuasive.

First, Adkisson clearly show in figure 2 that the second semiconductor layer 20 is adjacent the semiconductor structure (thin vertical Si region) and has a first semiconductor portion which is adjacent the first sidewall and having a fist non-horizontal surface (vertical surface of gate polysilicon sandwiching the gate oxide with the semiconductor structure) and a third semiconductor portion which is adjacent the second sidewall and having a second non-horizontal surface (vertical surface of gate polysilicon sandwiching the gate oxide with the semiconductor structure). Adkisson does not clearly depict the second semiconductor layer having a second semiconductor

portion over the semiconductor structure. Nonetheless, this limitation is still taught by Adkisson. To recognize that this limitation is taught, one needs to look at the entirety of the process Adkisson performs to obtain the structure shown in figure 2.

Adkisson teach on column 3 lines 41-48 that the gate material (polysilicon) 20 is deposited, polished and recessed below the nitride 16 surface. Figure 2 shows the resulting structure after all three steps have been completed, that is after depositing, polishing and recessing the polysilicon gate material. As explained in the rejection, at an intermediate point not shown in the figures after the deposition and before the polishing and recessing steps, the second semiconductor layer 20 has a second portion that is over the semiconductor structure. One of ordinary skill in the art would recognize that the deposition step initially forms the second semiconductor layer 20 over the entire structure. This deposition would result in a structure where the second semiconductor layer 20 has a portion over the semiconductor structure. This deposition would be similar to the conventional deposition of polysilicon 18 as shown in figure 2B of Fried et al. (see paragraph 0029 of Fried et al. for a brief discussion of the "conventional" deposition of the polysilicon). The end result of this deposition process gives the structure of the second semiconductor layer as claimed. If the deposition process did not result in this structure having the second semiconductor including a second portion above the semiconductor structure, then the polishing step of Adkisson could not be performed. Adkisson teach in column 3 lines 45-47 that in the polishing step the nitride serves as a polish stop. Thus, one of ordinary skill in the art would recognize that the second semiconductor material 20 would necessarily be formed elevated above the

semiconductor structure (and nitride cap on the semiconductor structure) in order for the polishing to be performed as taught using the nitride as a polish stop. Thus, in an intermediate point in the process, after the deposition but before the polishing and recessing, Adkisson teach the second semiconductor layer having the structure as recited in claim 17.

Appellant further argues that there is no teaching in Adkisson of "doping the first semiconductor portion with a first species," "doping the third semiconductor portion with a second species opposite the first species" or of teaching that the double gates are oppositely doped in conductivity. This argument is not persuasive. Adkisson is not relied upon to teach these claimed features. These steps are taught by Fried and have been properly combined with Adkisson to result in the invention as recited in claim 17. Thus, Adkisson's lack of teaching these features is not persuasive in arguing against the rejection based upon Adkisson in view of Fried. This argument merely attacks Adkisson individually. Nonobviousness cannot be shown by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the combination of Adkisson with Fried as applied and explained in the rejection above, Adkisson with Fried do teach doping the first semiconductor portion with a first species and doping the third semiconductor with a second species opposite the first species that results in the double gates being oppositely doped in conductivity.

Appellant further states that there is no teaching or suggestion of using a semiconductor structure for "preventing migration of doping species between the first gate region and the second gate region" as recited in claim 17. This is not persuasive. Though not explicitly recognized by Adkisson or Fried alone, the end result of the combination of their processes (using the first and second opposite conductivity implants of Fried into the process of Adkisson) is that the semiconductor structure prevents migration of the doping species between the first and second gates. Since Adkisson teach removing the portion of the gate material (second portion of the second semiconductor layer 20) over the semiconductor structure to separate the layer into a first and second gate, the net result is the same as that claimed where the semiconductor structure (which exists between and separates the two gates) prevents the migration of the doping species.

Appellant further argues that Fried et al. do not teach or suggest "removing a portion of the conductive layer and the second semiconductor layer to physically separate a first gate region and a second gate region." This argument is not persuasive since the rejection over the combination of Adkisson with Fried does not rely upon Fried to teach this limitation. Adkisson teach removing a portion of the conductive layer in figures 3, 3a, 5 and 5a as well as in column 3 lines 61 through column 4 line 24 and column 4 lines 65 through column 5 line 12. Adkisson teach removing a portion of the second semiconductor layer to physically separate a frist gate region and a second gate

region to arrive at the structure of figure 2 in column 3 lines 40-49. Thus, even though Fried does not teach these steps, they are taught by Adkisson in the rejection over the combination of references. This argument merely attacks Fried individually. Nonobviousness cannot be shown by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant further argues that Fried does not teach or suggest "the semiconductor structure preventing migration of doping species between the first gate region and the second gate region." This is not persuasive. Though not explicitly recognized by Adkisson or Fried alone, the end result of the combination of their processes (using the first and second opposite conductivity implants of Fried into the process of Adkisson) is that the semiconductor structure prevents migration of the doping species between the first and second gates. Since Adkisson teach removing the portion of the gate material (second semiconductor layer 20) over the semiconductor structure to separate the layer into a first and second gate, the net result is the same as that claimed where the semiconductor structure (which exists between and separates the two gates) prevents the migration of the doping species.

Appellant then argues that Adkisson and Fried combined have no teaching or suggestion to prevent the cross-migration of a FINFET having asymmetric gate doping

and that any statement saying so is hindsight reconstruction. This is not persuasive. Neither Adkisson nor Fried need to have a teaching or suggestion to prevent the cross-migration. This feature is a necessary function of the necessary result of the combination of Adkisson and Fried. Adkisson and Fried have been properly combined, using teachings and motivations from the references themselves, to obtain the claimed invention. The fact that neither reference recognizes the problem of cross-migration does not refute the fact that the structure obtained by their combination does prevent the cross-migration.

Appellant further argues that applying the angle implanting of Fried to the structure of Adkisson in figure 2 or 3 would not result in gate regions having a single dopant type. This is not persuasive. This argument is based upon the teaching of Fried that horizontal portions of the gate structure will not be shadowed during either the first or second implant and will thus receive both implants and that since figure 2 of Adkisson only has a horizontal gate structure it will be double implanted. First, as explained in the rejection, it would have been obvious to one of ordinary skill in the art to employ the angled implant of Fried to the intermediate structure of Adkisson after depositing the second semiconductor layer and before polishing and recessing. One would be motivated to employ the implantation of Fried at this point in the process to obtain the advantageous asymmetric gates of Fried. Employing the angled implantation of Fried at the further point in the process shown in Adkisson figure 2 (after polishing and recessing) would ignore the teachings of Fried in using the angled implant specifically to

obtain oppositely doped gates. Note that appellant argues that applying the implant of Fried to the structure of Adkisson figure 2 or 3 would not result in the gate regions having a single dopant type. The examiner does not refute this point. However, the rejection relies upon applying the implant of Fried in Adkisson's process before figure 2, at which point the angled implant will produce the claimed gates. Thus, appellant's argument is not persuasive.

Dependent Claims 18-21 and 23-25

Appellant does not present any further arguments for these dependent claims. The arguments made with regard to claim 17 above apply to these dependent claims and the arguments and the rejection they are in support of are considered proper.

Independent Claim 34

Independent claim 34 was rejected in a similar manner to claims 1 and 17 using Adkisson in view of Fried. Appellant does not present any new arguments with regard to claim 34 that has not already been responded to above. Note that the language of claim 34 is slightly different than claims 1 and 17 above. However, the same logic and reading of the references applied in the proper rejection of claim 34.

Response to the Argument for Ground 2:

Dependent Claim 15

Appellant argues that the dual-gated transistor structures described by Forbes is otherwise significantly dissimilar to the structure claimed in claim 15 by having physically separate and mirrored gates overlying the same channel region. This argument is not well understood. The rejection of claim 15 merely relied upon Forbes to teach annealing a doped gate region (463a) and a second electrode region (463b) before forming a metal (560) in order to activate the dopant species in the gate layer. Forbes is considered relevant art to Adkisson and Fried since Forbes also teaches forming semiconductor transistors. Thus, the combination of Adkisson with Fried and Forbes is considered proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

N. Drew Richards

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Conferees:

Tom Thomas

Darren Schuberg